In the Claims

1. (currently amended) A receive circuit comprising:

[[a.]] a data input terminal ~~adapted~~ to receive a stream of input data;

~~b. a first clock node adapted to receive a first clock signal;~~

~~c. a second clock node adapted to receive a second clock signal;~~

[[d.]] a first sampler having a first sampler data terminal coupled to the data input terminal, a first clock terminal ~~coupled to the first clock node~~, and a first data output terminal;

[[e.]] a second sampler having a second sampler data terminal coupled to the data input terminal, a second clock terminal ~~coupled to the second clock node,~~ and a second data output terminal;

[[f.]] a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node coupled to the second data output terminal, and a comparison-circuit output node; and

[[g.]] a multiplexer having a first multiplexer input terminal coupled to the first data output terminal, a second multiplexer input terminal connected to the [[third]] second data output terminal, a select terminal, and a multiplexer output terminal.

2. (original) The receive circuit of claim 1, wherein the data input terminal, the first sampler, the second sampler, and the comparison circuit are disposed on a semiconductor chip.

3. (original) The receive circuit of claim 1, wherein the first and second samplers sample the stream of input data to produce respective first and second sampled-data streams, and wherein the comparison circuit is adapted to compare at least one of the sampled-data streams with expected data.

4. (original) The receive circuit of claim 1, wherein the comparison circuit issues an error signal in response to mismatches between the first and second sampled-data streams.

5. (original) The receive circuit of claim 4, wherein the comparison circuit issues an error signal in response to each mismatch between the first and second sampled-data streams.

6. (previously presented) The receive circuit of claim 1, further comprising clock control circuitry coupled to the second clock terminal and to provide the second clock signal, wherein the clock control circuitry is adapted to vary the phase of the second clock signal in response to a timing control signal.

7. (original) The receive circuit of claim 6, wherein the clock control circuitry varies the phase of the first clock signal in response to a second timing control signal.

8. (original) The receive circuit of claim 1, further comprising a third sampler having a third sampler data terminal coupled to the data input terminal, a third clock terminal, and a third data output terminal.

9. (canceled)

10. (previously presented) The receive circuit of claim 1, wherein the first multiplexer input terminal is coupled to the first data output terminal via the comparison circuit.

11. (previously presented) The receive circuit of claim 1, wherein the first comparison circuit input node is coupled to the multiplexer output terminal and the first multiplexer input terminal is coupled to the first data output terminal.

12. (currently amended) A method comprising:

[[a.]] sampling a series of input symbols using a [[first]] clock signal of a [[first]] clock phase to produce a [[first]] series of sampled symbols;

~~b. sampling the series of input symbols using a second clock signal of a second clock phase to produce a second series of sampled symbols; and~~

[[c.]] comparing sampled symbols of the [[first]] series of sampled symbols with expected data to identify mismatches between the symbols and the expected data ~~corresponding sampled symbols of the second series of sampled symbols~~;

matching the series of sampled symbols with a data pattern; and

issuing an error signal responsive to the mismatches only if the series of sampled-data symbols matches the data pattern

~~d. wherein the series of input symbols are sampled using the first clock phase at a first sample voltage and using the second clock phase at a second sample voltage.~~

13. (currently amended) The method of claim 12, further comprising adjusting, in response to the ~~comparing~~ error signal, at least one of the clock phase or a sample voltage ~~first and second clock phases with respect to the other of the first and second clock phases~~.

14. (original) The method of claim 12, wherein the sampling and comparing are completed on a semiconductor chip.

15. (canceled)

16. (currently amended) The method of claim 12, wherein the series of input signals are sampled with respect to a sample voltage, the method further comprising adjusting the sample voltage responsive to the error signal ~~at least one of the first and second sample voltages with respect to the other of the first and second sample voltages in response to the comparing~~.

17. (currently amended) The method of claim 12, further comprising sampling the series of input signals using a second clock signal of a second clock phase to obtain the expected data ~~issuing an error signal in response to a mismatch between ones of the first and second series of sampled symbols~~.

18. (currently amended) The method of claim [[12]] 17, further comprising storing phase offsets between the first-mentioned clock phase and the second clock phase ~~wherein the comparing produces error data for a plurality of phase offsets between the first and second clock phases, the method further comprising storing the error data~~.

19. (currently amended) The method of claim 18, further comprising relating the stored phase offsets with the error signals ~~storing information regarding each of the phase offsets and the corresponding error data~~.

20. (currently amended) The method of claim [[18]] 19, further comprising calculating a timing margin using the stored phase offsets and the error signals ~~error data~~.

21. (currently amended) The method of claim 18, wherein the series of input symbols are sampled using the first-mentioned clock phase at a first sample voltage and using the second clock phase at a second sample voltage, and wherein the comparing produces a second error signal [[data]] for a plurality of voltage offsets between the first and second sample voltages.

22. (currently amended) The method of claim 21, further comprising plotting first error data derived from the first-mentioned error [[data]] signal and second error data derived from the second error signal [[data]].

23. (currently amended) A method comprising:

[[a.]] sampling a series of data symbols using a [[first]] sample voltage to produce a [[first]] series of sampled-data symbols;

~~b. sampling the series of data symbols using a second sample voltage to produce a second series of sampled-data symbols; and~~

[[c.]] comparing ~~corresponding ones of the first and second~~ the series of sampled-data symbols with expected data to identify mismatches between the sampled-data symbols and the expected data;

matching the series of sampled symbols with a data pattern; and

issuing an error signal responsive to the mismatches only if the series of sampled-data symbols matches the data pattern

~~d. wherein the series of data symbols are sampled using a first clock signal of a first clock phase and using a second clock signal of a second clock phase~~.

24. (currently amended) The method of claim 23, further comprising adjusting ~~at least one of the first and second sample voltages~~ the sample voltage responsive to the error signal ~~with respect to the other of the first and second sample voltages~~.

25. (original) The method of claim 23, wherein the sampling and comparing are completed on a semiconductor chip.

26. (canceled)

27. (currently amended) The method of claim 23, wherein the series of data symbols are sampled at a clock phase, the method further comprising adjusting the clock phase responsive to the error signal ~~at least one of the first and second clock phases with respect to the other of the first and second clock phases in response to the comparing~~.

28. (currently amended) The method of claim 27, further comprising storing information regarding the sample voltage and the clock phase ~~first and second sample voltages and the first and second clock phases~~.

29. (original) The method of claim 28, further comprising calculating a timing margin using the information.

30. (original) The method of claim 29, further comprising plotting the information.

31. (currently amended) A method comprising:
    a. sampling a series of data symbols using a first sample voltage to produce a first series of sampled-data symbols;
    b. sampling the series of data symbols using a second sample voltage to produce a second series of sampled-data symbols; and
    c. identifying mismatches between ~~comparing corresponding~~ ones of the first and second series of sampled-data symbols for a selected pattern of the data symbols;

d. wherein the series of data symbols are sampled using a first clock signal of a first clock phase and using a second clock signal of a second clock phase~~; and~~

~~e. wherein comparing corresponding ones of the first and second series of sampled-data symbols generates includes comparing only a subset of the first and second series of sampled-data symbols.~~

32. (currently amended) A method comprising:

[[a.]] sampling a series of data symbols using a first sample voltage to produce a first series of sampled-data symbols;

[[b.]] sampling the series of data symbols using a second sample voltage to produce a second series of sampled-data symbols;

[[c.]] comparing corresponding ones of the first and second series of sampled-data symbols; and

[[d.]] matching the first series of sampled-data symbols to at least one data pattern; and issuing a pattern-specific error signal if corresponding ones of the symbols in the first and second series of sampled-data signals mismatch when the first series of sampled-data symbols matches the data pattern.

33. (canceled)

34. (previously presented) A communication system comprising:

a. a transmitter to transmit a series of data symbols; and

b. a receive circuit including:

i. a data input terminal to receive the series of data symbols;

ii. a first clock node to receive a first clock signal;

iii. a second clock node to receive a second clock signal;

iv. a first sampler having a first sampler data terminal coupled to the data input terminal, a first sampler clock terminal coupled to the first clock node, and a first data output terminal;

v. a second sampler having a second sampler data terminal coupled to the data input terminal, a second sampler clock terminal coupled to the second clock node, and a second data output terminal; and

vi. a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node coupled to the second data output terminal, and a comparison-circuit output node; and

vii. a data filter having a first data-filter input terminal coupled to at least one of the first and second sampler output terminals and a second data-filter input terminal coupled to the comparison-circuit output node.

35. (original) The communication system of claim 34, wherein the first and second samplers and the comparison circuit are disposed on a first semiconductor chip.

36. (original) The communication system of claim 35, wherein the transmitter is disposed on a second semiconductor chip.

37. (canceled)

38. (previously presented) A communication system comprising:

a. a transmitter adapted to transmit a series of data symbols; and

b. a receive circuit including:

i. a data input terminal adapted to receive the series of data symbols;

ii. a first clock node adapted to receive a first clock signal;

iii. a second clock node adapted to receive a second clock signal;

iv. a first sampler having a first sampler data terminal coupled to the data input terminal, a first sampler clock terminal coupled to the first clock node, and a first data output terminal;

v. a second sampler having a second sampler data terminal coupled to the data input terminal, a second sampler clock terminal coupled to the second clock node, and a second data output terminal; and

vi. a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node

coupled to the second data output terminal, and a comparison-circuit output node; and

c. a data filter having a first data-filter input terminal coupled to at least one of the first and second sampler output terminals and a second data-filter input terminal coupled to the comparison-circuit output node;

d. wherein the data filter includes a pattern-matching circuit that compares sampled data from the first data output terminal with a data pattern.

39. (previously presented) The communication system of claim 38, wherein the data filter conveys sampled error symbols on the comparison-circuit output node when the sampled data matches the data pattern.

40. (currently amended) A receiver comprising:

a. a data input terminal to receive a stream of input data;

b. a first clock node to receive a first clock signal;

c. a second clock node to receive a second clock signal;

d. first sampling means having a first sampler data terminal coupled to the data input terminal, a first clock terminal coupled to the first clock node, and a first data output terminal;

e. second sampling means having a second sampler data terminal coupled to the data input terminal, a second clock terminal coupled to the second clock node, and a second data output terminal;

f. error-detection means coupled to the first and second data output terminals and having an error-detection output node to provide an error signal; and

g. a data filter having a first data-filter input terminal coupled to at least one of the first and second sampler output terminals and a second data-filter input terminal coupled to the ~~comparison-circuit~~ error-detection output node to receive the error signal.

41. (original) The receiver of claim 40, wherein the first and second sampling means sample the stream of input data to produce respective first and second sampled-data streams.

42. (currently amended) The receiver of claim 41, wherein the error-detection means ~~comparison circuit~~ issues [[an]] the error signal in response to mismatches between the first and second sampled-data streams.

43. (currently amended) The receiver of claim 42, wherein the comparison circuit issues [[an]] the error signal in response to each mismatch between corresponding data symbols in the first and second sampled-data streams.

44. (canceled)

45. (currently amended) A receiver comprising:
    a. a data input terminal adapted to receive a stream of input data;
    b. a first clock node adapted to receive a first clock signal;
    c. a second clock node adapted to receive a second clock signal;
    d. first sampling means having a first sampler data terminal coupled to the data input terminal, a first clock terminal coupled to the first clock node, and a first data output terminal;
    e. second sampling means having a second sampler data terminal coupled to the data input terminal, a second clock terminal coupled to the second clock node, and a second data output terminal;
    f. error-detection means coupled to the first and second data output terminals and having an error node to issue error signals; and
    g. a data filter having a first data-filter input terminal coupled to at least one of the first and second sampler output terminals and a second data-filter input terminal coupled to the ~~comparison-circuit output~~ error node to receive the error signals;
    h. wherein the data filter includes a pattern-matching means for comparing sampled data from the first data output terminal with a data pattern.

46. (currently amended) The receiver of claim 45, wherein the data filter conveys ~~sampled data symbols on the comparison-circuit output node~~ the error signals when the sampled

data matches the data pattern.

47. (new) A method comprising:

receiving an input signal;

sampling the input signal at a first phase and with respect to a first reference to provide a first series of sampled symbols;

sampling the input signal at a second phase and with respect to a second reference to provide a second series of sampled symbols;

while equalizing the input signal responsive to the second series of sampled symbols: adjusting at least one of the first phase and the first reference over a range of values; comparing respective symbols in the first and second series of sampled symbols for the range of values to identify symbol mismatches; and correlating the mismatches with values in the range of values to recover margin information;

deriving a sample point from the margin information;

setting at least one of the first phase and the first reference to the sample point; and

sampling the input signal at the sample point.

48. (new) The method of claim 47, further comprising comparing the second series of sampled data with a data pattern and deriving the sample point from the margin information recovered when the data pattern matches the second series of sampled data.

49. (new) A receiver comprising:

a sampler to sample a series of input symbols at a sample phase and with respect to a reference to recover a series of sampled symbols;

an expected-data source to provide a series of expected symbols;

a comparison circuit having a first comparison-circuit input node coupled to the sampler to receive the recovered series of sampled symbols and a second comparison-circuit input node coupled to the expected-data source to receivc the series of expected symbols, the comparison circuit to identify mismatches between corresponding symbol pairs in the sampled and expected symbols;

a filter having a pattern-matching circuit to compare the expected symbols with a pattern and to assert an error signal if the mismatches occur when the expected symbols match the pattern.

50. (new) The method of claim 48, wherein the expected-data source comprises a second sampler to sample the series of input symbols.